

**DESIGN AND SYNTHESIS OF EFFICIENT MAC ARCHITECTURES FOR HIGH SPEED DECIMAL PROCESSOR**

**ABSTRACT**

The work focuses on the design and synthesis of efficient decimal MAC (Multiply Accumulate) architecture for high speed decimal processors based on IEEE 754-2008 Standard for Decimal Floating Point (DFP) Arithmetic. The design makes use of Binary Coded Decimal (BCD) coding for decimal representation. The decimal MAC unit has a DFP multiplier fused with a DFP adder module. This research presents two novel techniques for iterative DFP multiplication. The first approach has a Decimal Fixed Point (DFxP) multiplier using a novel Double Digit Decimal Multiplication (DDDM) technique that performs two digit multiplications simultaneously. The second approach does DFxP multiplication using a novel RPS algorithm. In this approach partial products for column accumulation are generated from the least significant end in an iterative manner using BCD digit multipliers. A novel design for BCD digit multiplication that reduces the critical path delay and area is also proposed in this research. The research also presents parallel DFP multiplier having parallel DFxP multiplier for significand digit multiplication. Different designs of DFP adders are also implemented aiming at reducing the delay. Improved designs for reversible logic implementation of BCD adder that are highly optimized in terms of number of reversible gates and garbage outputs are presented. This research also presents an approach to obtain reduced hardware and/or delay for synthesizing logic functions using multiplexers. A design using only one type of modular building blocks can decrease system design and manufacturing cost for MAC implementation.

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